# NICKEL SALICIDE PROCESS WITH REDUCED DOPANT DEACTIVATION

## CROSS REFERENCE TO RELATED APPLICATION

[0001]    This application claims priority under 35 U.S.C. § 119 from Korean

Patent Application Nos. 2003-24126, filed on April 16, 2003, and 2003-42838, filed

on June 27, 2003, in the Korean Intellectual Property Office, and under 35 U.S.C.

§ 120 as a continuation-in-part of U.S. Patent Application 10/726,638, filed December

4, 2003, the disclosures of which are hereby incorporated by reference in their entirety.

## BACKGROUND OF THE INVENTION

Field of the Invention

[0002]    The present invention relates to an improved method for fabricating

semiconductor devices and, more particularly, an improved method for forming

salicide structures during semiconductor device manufacturing processes using nickel,

a nickel alloy, or another metal or metal alloy capable of forming silicides at lower

temperatures, *e.g.*, less than about 725 °C., to form the salicide layer and modifying

the heat treatment sequence to reactivate previously deactivated dopant atoms.

Description of the Related Art

[0003]    As the integration density of semiconductor devices continues to

increase and the critical dimensions associated with such devices continue to decrease,

there has been a corresponding increase in interest in identifying materials and

processes for producing interest in low resistance materials to maintain or reduce

signal delay.  Silicide and salicide (self-aligned silicide) materials and processes have

been widely used to lower the sheet resistance and contact resistance for the gate conductor and source/drain regions of MOS devices.

[0004] A number of metals, including tungsten, tantalum, zirconium, titanium, hafnium, platinum, palladium, vanadium, niobium, cobalt, nickel and various alloys of such metals have been used to form silicide layers on semiconductor devices. For gate lengths below about 100 nm, however, conventional salicide processes and materials tend to experience a variety of difficulties including opens, residues and layer non-uniformity, resulting at least in part from agglomeration within the silicide material layer.

[0005] These difficulties tend to be exacerbated by the high-temperature processing required to react most metal(s) with silicon to form the desired silicide layers. The high temperature anneals required also raise concerns regarding the impact of the silicide annealing process(es) on the thermal budget for the devices being manufactured. For example, when cobalt is used to form the silicide, the initial stoichiometry of the silicide may be generally represented as CoSi, but as the annealing process continues, particularly at higher temperatures, the silicide tends to incorporate an increasing amount of silicon and approaches a composition more closely represented as $CoSi_2$. For devices having gate lengths below about 100 nm, however, the second high temperature silicidation used in conventional Co salicide processes tends to induce agglomeration within the silicide material layer, increasing the degree of non-uniformity within the layer and tending to degrade the performance of the resulting devices.

[0006] A conventional salicide process sequence is illustrated in FIG. 1, wherein, after forming a gate structure (S10), a first ion implant process is used to form a lightly-doped drain (S20), gate spacers are formed (S30) adjacent the gate

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electrode sidewalls, a heavier source/drain (S/D) implant (S40) is used to form the S/D regions in the substrate, and an activation anneal (S50) is conducted to activate a portion of the implanted dopant(s) to modify the performance of the implanted regions of the substrate. After the dopant activation anneal, a silicide blocking layer is formed (S60), a silicidation metal or metal alloy layer is formed and a salicide pattern is formed by reacting the silicidation metal(s) with exposed silicon surfaces, after which the remainder of the silicidation metal(s) are removed (S70). Once the salicide pattern has been formed, the unreacted portion of the silicidation metal(s) may be removed and an interlayer dielectric formed (S80) to begin the metallization process.

[0007]    Nickel is an attractive metal for forming silicides because the annealing process required to form the desired silicide may be conducted at a relatively low temperature, *e.g.*, below about 550 °C. Depending on the reaction conditions, nickel can react with silicon to form dinickel monosilicide, $Ni_2Si$, nickel silicide, $NiSi$, or nickel disilicide, $NiSi_2$, as the silicidation product. Using annealing temperatures greater than about 550 °C. tends to increase the formation of the most resistive nickel-disilicide $NiSi_2$ and a corresponding increase in the silicon consumption and are, therefore, generally avoided. Nickel silicide, $NiSi$, however, can be preferentially formed at lower temperatures and provides the lowest sheet resistance of the three nickel silicide phases. Due to the low silicidation temperature, $NiSi$ exhibits a decreased tendency to agglomerate and form a silicide layer in which the sheet resistance is generally independent of the device dimensions, increasing its utility for lowering the resistance of fine line structures.

## SUMMARY OF THE INVENTION

[0008]    Embodiments of the present invention provide methods of forming gate pattern, performing one or more dopant implants, typically a lightly-doped drain (LDD) implant, followed by gate spacer formation and a source drain (S/D) implant, forming a silicide blocking layer (SBL), activating (or reactivating) the dopant, depositing a silicidation metal or metal alloy and forming a silicide layer by reacting the metal or metal alloy with the exposed portions of the silicon at a silicidation temperature of less than about 700 °C., such as nickel and nickel/tantalum alloys, to produce a salicide pattern.

[0009]    When the heat processes associated with lower temperature SBL and salicide pattern formation, e.g., involving temperatures typically less than about 700 °C., the heat budget associated with the processes are reduced, allowing the formation of more highly integrated devices, however, these lower temperature processes are also associated with dopant deactivation that will tend to increase the resistance and threshold voltages of the resulting devices and reduce their performance accordingly.

[0010]    Exemplary methods of forming such lower temperature nickel silicide layers may include forming a capping layer of a material such as titanium nitride, TiN, and particularly a nitrogen-rich TiN layer, i.e., a TiN layer having a N:Ti atomic ratio of at least about 0.5, on the nickel alloy layer prior to forming the silicide. The alloying metal selected should exhibit both a diffusivity and a solubility in silicon that are lower than the corresponding values for nickel. The alloying metal should also exhibit a silicidation temperature in excess of that necessary to form nickel silicide.

[0011]    Depending on the particular process flow used to prepare the substrate prior to the deposition of the metal or metal/alloy, metal silicides according

to the exemplary embodiments of the invention may be formed only on the gate electrode structure, only on the surface of active regions, *e.g.*, the source/drain regions of MOS transistors, or on both the gate electrode and the active regions.

[0012]    In those instances in which the metal silicide will not be formed on the gate electrode, the gate electrode structure will typically include one or more capping or SBL layers to protect any polysilicon layer incorporated in the gate electrode structure above the gate dielectric layer.  In those instances in which the metal silicide will be limited to the gate electrode, a sequence of insulator deposition, typically one or more layers of a chemical vapor deposition (CVD) oxide, can be formed on the substrate.  The upper portion of the insulator(s) may then be removed using, for example, a chemical-mechanical polishing or etchback process, to expose an upper silicon surface on the gate electrode structure while protecting the active regions from exposure to the metal or metal alloy.

[0013]    In each instance, a layer of a metal or metal alloy will be deposited on a substrate having regions with exposed silicon and/or polysilicon surfaces, typically ("Typically" does not mean to imply prior art.) followed by the deposition of an optional capping layer such as TiN.  A heat treatment, typically at a temperature of at least 250 °C. and typically less than 700 °C., will be used to react the metal or metal alloy with the exposed silicon surfaces to form the desired silicide.  The capping layer and the unreacted metal or metal alloy may then be removed to prepare the substrate for additional processing.

[0014]    When the primary silicidation metal is nickel, one or more alloying metals may be selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium, palladium and niobium, but the total content of the alloying metals will typically constitute no more than about 20 atomic

percent of the nickel alloy and *may be present at content levelsover 0.1 atomic*

*percent.* The nickel silicide formation will typically include heating the nickel alloy

in contact with a silicon surface to a temperature above about 200 °C. and below

about 700 °C., more typically between about 250 °C. and about 500 °C., for a period

of at least about 10 seconds and possibly for as long as 30 minutes or more. When

using a nickel alloy, particularly a nickel-tantalum alloy, the particular time and

temperature combination selected should preferably be sufficient to produce a two-

layered nickel silicide structure in which the majority of the nickel is present in the

lower layer as NiSi and the majority of the alloying metal has been segregated into the

upper layer.

[0015] Although the nickel silicides prepared according to the exemplary

embodiments of the present invention tend to exhibit higher thermal stability,

particularly at temperatures above about 600 °C., than nickel silicides prepared from

unalloyed nickel, the thermal activity of subsequent processes should generally be

selected to maintain the majority, typically at least 90%, of the lower layer of the

silicide in the initial NiSi phase, *i.e.*, suppress conversion of NiSi to $NiSi_2$, in the final

semiconductor device.

[0016] Nickel silicides prepared according to the exemplary embodiments

of the present invention exhibit performance improvements over both nickel silicides

prepared from unalloyed nickel and more conventional cobalt silicides, particularly

for devices incorporating gate structures below 100 nm and more particularly for

devices incorporating gate structures below 50 nm. In particular, nickel silicides

according to the present invention tend to exhibit lower and more stable sheet

resistance, both upon formation and particularly after additional thermal processing.

[0017] Similarly, devices incorporating nickel silicides according to the exemplary embodiments tend to exhibit improved threshold voltages $V_{th}$, reduced diode leakage currents, improved off-current $I_{doff}$ and saturation current $I_{dsat}$ performance over the performance provided by identical devices incorporating cobalt silicides, particularly in PMOS devices. The addition of a high tensile tension capping layer such as, for example, a SiON layer, particularly on NMOS transistors that incorporate the exemplary nickel silicides according to the invention can further improve NMOS device performance.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Exemplary embodiments of the devices and methods that may be utilized to practice the present invention are addressed more fully below with reference to the attached drawings in which:

[0019] FIG. 1 illustrates certain of the process steps in a conventional method for manufacturing semiconductor devices incorporating a salicide structure;

[0020] FIGS. 2A and 2B are graphs illustrating the temperature dependence of the deactivation and activation of dopants for NMOS and PMOS transistors;

[0021] FIG. 3A and 3B illustrates certain of the process steps according to two exemplary methods for manufacturing semiconductor devices incorporating a salicide structure according to the present invention;

[0022] FIGS. 4A-4G illustrate certain of the steps associated with the manufacture of semiconductor devices incorporating a salicide structure according to the exemplary embodiments of the invention;

[0023]    FIG. 4H is an enlarged illustration of a portion H of the silicide structure in a S/D region manufactured according to the method illustrated in FIG. 4A-F using a nickel/tantalum alloy as the silicidation metal;

[0024]    FIGS. 5A-B are graphs illustrating the threshold voltage $V_{th}$ variations in NMOS and PMOS transistors using $CoSi_2$ and $NiSi$ silicides;

[0025]    FIGS. 6A-B are graphs illustrating the sheet resistance distributions of N+ (S/D) and N- (LDD) doped regions as a function of the anneal/SBL sequence;

[0026]    FIGS. 7A-B are graphs illustrating the drain saturation current $I_{dsat}$ in NMOS and PMOS transistors using $CoSi_2$ and $NiSi$ silicides;

[0027]    FIGS. 8A-B are graphs illustrating the poly gate depletion effect for 500 °C. and 750 °C. SBL processes for NMOS and PMOS transistors;

[0028]    FIGS. 9A-B are graphs illustrating the $V_{th}$ variation according to gate length for NMOS and PMOS transistors using $CoSi_2$ and $NiSi$ silicides without an SBL process;

[0029]    FIGS. 10A-B are graphs illustrating the gate oxide capacitance-voltage (C-V) curves for NMOS and PMOS transistors using $CoSi_2$ and $NiSi$ silicides without an SBL process;

[0030]    FIGS. 11A-B are graphs illustrating the gate oxide capacitance-voltage (C-V) curves for NMOS and PMOS transistors using $NiSi$ silicide as a function of the presence and timing of activation anneals and an SBL process;

[0031]    FIGS. 12A-B are graphs illustrating the drain saturation current $I_{dsat}$ in NMOS and PMOS transistors using $NiSi$ silicide as a function of the presence and timing of activation anneals and an SBL process; and

[0032]    FIGS. 13A-B are graphs illustrating the drain saturation current $I_{dsat}$ in NMOS and PMOS transistors using various Co and Ni silicides manufactured using the SBL skip process.

[0033]    These drawings are provided to assist in the understanding of the exemplary embodiments of the invention as described in more detail below and should not be construed as unduly limiting the invention.  The relative spacing, sizing and dimensions of the various elements illustrated in the drawing are not drawn to scale and may have been exaggerated, reduced or otherwise modified for the purpose of improved clarity.  Those of ordinary skill in the art will also appreciate that certain layers that may be commonly utilized in the manufacture of semiconductor devices including, for example, photoresist patterns and multilayer metallization structures, have been omitted simply to improve clarity and reduce the number of drawings.

## DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0034]    As illustrated in FIG. 3A, an exemplary method of forming a semiconductor device according to the present invention will include the steps of forming a gate pattern, S110, forming a lightly-doped drain (LDD) using the gate pattern as the implant mask, S120, forming spacer structures adjacent the sidewalls of the gate pattern, S130, forming the source/drain regions using the gate pattern and the spacer structures as the implant mask, S140, forming a silicide blocking layer (SBL), S150, performing a dopant activation anneal, S160, forming a salicide pattern, S170, and forming an interlayer dielectric (ILD), S180, to begin the metallization process by which the active devices are connected to each other and external contacts.  The silicidation process may include sequentially depositing a nickel alloy and a titanium

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nitride layer, heating to a temperature sufficient for the nickel alloy to form a silicide with the exposed silicon surfaces.

[0035] As illustrated in FIG. 3B, another exemplary method of forming a semiconductor device according to the present invention will include the steps of forming a gate pattern, S210, forming a lightly-doped drain (LDD) using the gate pattern as the implant mask, S220, forming spacer structures adjacent the sidewalls of the gate pattern, S230, forming the source/drain regions using the gate pattern and the spacer structures as the implant mask, S240, performing a first dopant activation anneal, S250, forming a silicide blocking layer (SBL), S260, performing a post-SBL anneal anneal, S270, forming a salicide pattern, S280, and forming an interlayer dielectric (ILD), S290, to begin the metallization process by which the active devices are connected to each other and external contacts.

[0036] As illustrated in FIG. 4A, a semiconductor device may be formed in a substrate 51 on which or into which isolation regions 53 are formed to define an active region using a conventional shallow-trench isolation (STI) process. As illustrated, a gate structure including a gate insulator layer 55, a gate electrode 57, which may include a first conductor layer, such as doped polysilicon, a barrier layer, such as tungsten nitride, a second conductor layer, such as tungsten, and, optionally, a capping layer, may be formed in the active region. Using the gate structure as an implant mask, a first ion implant process may be used to form a lightly doped region 59, such as a lightly-doped drain region near the surface of the exposed regions of the active region.

[0037] As illustrated in FIGS. 4B-C, sidewall structures may then be formed adjacent the vertical surfaces of the gate structure using a conventional process involving the deposition of one or more insulating layers, which may include

a first material 61, typically silicon oxide, and a second material 63, typically silicon nitride, followed by an etchback process to form spacer 64 from the remaining portions 61a and 63a of the silicon oxide and silicon nitride layers. Using the gate electrode 57 and sidewall structures 64 as an implant mask, a second ion implant may be used to deposit a heavier concentration of dopant 65 into the exposed regions of the active region to complete the formation of the device source/drain regions adjacent the gate electrode.

[0038] As illustrated in FIG. 4D, a silicide blocking layer (SBL) 70, *typically*comprising a silicon oxide layer 67 and a silicon nitride layer 69, is then formed on the substrate to protect those regions other than the active regions, particularly those regions dedicated to the formation of elements, such as resistors utilized in electrostatic discharge (ESD) protection circuits, that require a higher sheet resistance to operate properly. Although illustrated as a combination of silicon oxide and silicon nitride, the SBL may be formed from a single material, such as silicon nitride, or combinations of other suitable materials as desired. The layer(s) comprising the SBL may be deposited using a chemical vapor deposition (CVD) process, typically at a temperature between about 535 °C. and about 825 °C. For example, CVD silicon nitride may be formed at about 700 °C.

[0039] However, at the process temperatures typically used during the formation of the SBL, a portion of the dopant impurities present in the gate electrode structure 57a, typically phosphorus-doped polysilicon, the LDD region 59a and the S/D regions 65a tend to be deactivated. The deactivation of these dopants will tend to increase the resistance of the doped regions, increase the junction leakage and reduce the gate capacitance, all changes that tend to degrade the performance of the resulting semiconductor devices.

[0040]     As illustrated in FIG. 4E, after the SBL has been formed, the

substrate may be subjected to a post-SBL anneal to activate or reactivate a portion of

the inactive or deactivated dopant species and form reactivated gate electrode

structures 57b, LDD regions 59b and S/D regions 65b that exhibit correspondingly

improved resistance, leakage and capacitance.  The post-SBL anneal may be

conducted using a rapid thermal process (RTP), also known as rapid thermal anneal

(RTA), at a temperature from about 830 °C. to about 1150 °C., typically about

1000 °C to about 1100 °C .  The post-SBL anneal will preferably be conducted under

a non-oxidizing atmosphere, typically in an $N_2$ gas ambient, although other inert gases

such as Ar or gas mixtures may be used.  In addition to the RTP process, the post-

SBL anneal may be conducted with any suitable heating process including, for

example, laser annealing, spike annealing and flash annealing.

[0041]     As illustrated in FIG. 4E, the substrate is typically treated with a HF

solution and possibly other substances to remove any native oxide that has formed on

the exposed silicon surfaces.  After the silicon surfaces have been cleaned, a layer of a

silicidation metal or metal alloy 71, such as a nickel/tantalum alloy, and preferably a

capping layer (not shown), such as titanium nitride, may then be formed over the

reactivated gate structure, LDD and source/drain regions and isolation regions.  When

forming a nickel silicide, the device may then be annealed at a temperature, typically

between about 400 °C. and about 530 °C., and preferably at least above 450 °C., and

for a time period sufficient to cause the metal or metal alloy layer 30 to react with the

exposed silicon of the active region and form a silicide region 71b and/or the gate

electrode region and form a silicide region 71a using, for example a rapid thermal

anneal (RTP) process.  In particular, when forming a nickel silicide, it is preferred

that the silicidation temperature not exceed about 550 °C. to suppress formation of the

more resistive tertiary nickel silicide $NiSi_2$ in favor of the less resistive secondary nickel silicide NiSi.

[0042]    Depending on the silicidation metal or metal alloy utilized, the silicidation temperature will be adjusted accordingly to ensure both that the desired silicide is formed substantially completely and that the thermal budget contribution of this process is not excessive.  Because the formation of the silicide is largely or completely confined to those regions in which a silicon surface was intentionally exposed prior to the deposition of the nickel alloy 30, the silicide formation will be considered a self-aligned silicide (salicide).

[0043]    As illustrated in FIG. 4G, the capping layer (not shown), if used, and the unreacted portion of the metal or metal alloy layer 71 may be removed using, for example, a solution including sulfuric acid, $H_2SO_4$, and hydrogen peroxide, $H_2O_2$, leaving the silicide regions 71a, 71b on the surface of the gate electrode and source/drain regions within the active region respectively.   An interlayer dielectric layer (ILD) 73 may be formed over the substrate.  Although illustrated as a single layer, those of ordinary skill in the art will appreciate that the ILD 73 may include more than one layer, more than one material and may be subjected to additional processing such as chemical-mechanical polishing or etchback processing to improve the planarity of the resulting surface.  Contact openings (not shown) in the ILD and metal patterns (not shown) may then be formed using a wide variety of conventional and/or proprietary deposition, etch and metallization processes and materials to provide the electrical connections to the transistors and other circuit elements necessary to produce a functional device.

[0044]    As illustrated in FIGS. 4E-G, if the composition of the gate structure is such that a silicon surface is exposed during the deposition of the metal or

metal alloy layer, a silicide may be formed at the upper surfaces of both the source

drain regions and the gate electrode. However, those of ordinary skill in the art will

appreciate that by modifying the structure illustrated in FIG. 4D through the use of the

SBL or a combination of other process steps suitable for forming a barrier layer or

layers, it is possible to form the silicide regions selectively in only the S/D regions or

on the gate electrode. For example, if the gate electrode structure 57 is manufactured

to include a doped polysilicon layer surrounded by one or more barrier or capping

layers, the formation of a silicide region on the gate electrode may be suppressed,

resulting in selective formation in only the exposed source/drain regions.

[0045]    As illustrated in FIG. 4H, which represents the region H indicated in

FIG. 4G, when certain metals and metal alloys are used in the silicidation process, for

example nickel-tantalum alloys, the silicidation process will produce a two-layered

silicide structure in which the primary metal may be preferentially segregated into a

lower layer $71a_L$ with the alloying metal remaining primarily in the upper layer $71a_U$.


Experimental Data

[0046]

[0047]    To study the effect of dopant deactivation on transistor, Vth of long

channel transistors are monitored for different additional annealing performed

between dopant activation and salicide process. (No SBL process is applied) . As

illustrated in FIGS. 2A and 2B, however, when semiconductor devices are processed

according to the conventional process illustrated in FIG. 1, the temperatures

experienced during processing subsequent to the activation anneal may affect the

performance of the resulting devices. In particular, processes such as the formation of

a silicon blocking pattern during which the process temperature does not exceed about

700 °C., a portion of the activated dopant species will tend to deactivate, thereby tending to increase both the resistance of the implanted regions and the threshold voltage of the affected transistors. This dopant deactivation, therefore, both tends to reduce the speed and decrease the current carrying capabilities of the resulting devices, thereby tending to degrade the operational performance, and perhaps functionality, of the resulting devices. In the case of cobalt salicidation, dopant can be reactivated at S70 of Fig.1. because cobalt salicidation is performed at about 850 °C. But in case of nickel salicidation, dopant can not be reactivated at S70 of Fig.1. because nickel salicidation is performed at less than 500 °C.

[0048]    In order to demonstrate the utility and effectiveness of the present invention, a number of NMOS and PMOS transistors and gate oxide capacitors were prepared using both conventional processes and materials, modified conventional processes, and exemplary processes and materials according to the present invention. Various evaluations were then conducted to collect data regarding threshold voltage, $V_{th}$, drain saturation current, $I_{dsat}$, and capacitance-voltage, C-V, and sheet resistance, $R_s$, performance as a function of the materials and processes utilized.

[0049]    As illustrated in FIGS. 5A-B, when employing a conventional process according to FIG. 1 in which the silicidation process occurs after the SBL formation, those metals and metal alloys that utilize a higher silicidation temperature, such as Co (plotted as $\triangle$) with its silicidation temperature in excess of about 750 °C., the dopant that was deactivated during the SBL process is reactivated. Those silicidation processes, however, that utilize a metal or metal alloy having a lower silicidation temperature, such as nickel or a nickel alloy (plotted as $\circ$) processed below about 530 °C., there tends to be no reactivation and indeed, depending on the temperature, may be further deactivation, of the dopants. The impact of the

silicidation temperature is reflected in the graphs presented as FIGS. 5A and 5B, showing the increase in threshold voltage $V_{th}$ in both NMOS and PMOS devices associated with the lower temperature silicidation process used to form NiSi as opposed to the higher temperature silicidation process used to form $CoSi_2$.

[0050]    As illustrated in FIGS. 6A-B, the dopant deactivation associated with SBL formation after the activation anneal (plotted as ○), if not remedied by a later reactivation anneal (plotted as □) performed after the SBL formation, will tend to increase both the magnitude and the variation in the sheet resistance $R_s$ of the underlying LDD and S/D regions.  This increased resistance, if uncorrected, will tend to reduce the speed of the resulting devices and to reduce the saturation currents that can be obtained.

[0051]    As illustrated in FIGS. 7A-B, when employing a process generally corresponding to the conventional process illustrated in FIG. 1, NMOS and PMOS devices utilizing a $CoSi_2$ silicide (plotted as ▲) demonstrate higher saturation drain current, $I_{dsat}$, values than those obtained using a lower temperature silicide, specifically NiSi (plotted as ○ and □).  When evaluated at a drain current off, $I_{doff}$, value of 10nA, the NMOS transistors illustrate a degradation in $I_{dsat}$ of about 8%.  A similar evaluation of the PMOS transistors reveals a degradation of about 5% or less, due probably in part to the improved conductivity provided by the silicide.

[0052]    As illustrated in the capacitance-voltage curves in FIGS. 8A-B, when employing a conventional process according to FIG. 1 in which the silicidation process occurs after the SBL formation, those metals and metal alloys that utilize a higher silicidation temperature, such as Co  (plotted as Δ) with its silicidation temperature in excess of about 750 °C., at least a portion of the dopant that was deactivated during the SBL process can be reactivated.  Those silicidation processes,

however, that utilize a metal or metal alloy having a lower silicidation temperature, such as nickel or a nickel alloy (plotted as $\circ$) processed at silicidation temperatures below about 530 °C., in this instance about 500 °C., there tends to be little or no reactivation and indeed, depending on the temperature, there may even be further deactivation, of the dopants. The impact of the post-SBL silicidation temperature is reflected in the graphs presented as FIGS. 8A and 8B, showing, in region A, the decrease in gate capacitance in both NMOS and PMOS devices associated with the lower temperature silicidation process used to form NiSi as opposed to the higher temperature silicidation process used to form $CoSi_2$. As reflected in FIGS. 8A and 8B, the deactivation of the dopant(s) by the SBL process decreased the gate oxide C-V inversion capacitance by about 10%.

[0053]    As illustrated in FIGS. 9A-B, when employing a conventional process generally according to FIG. 1, but without performing the SBL step, there is very little difference in the threshold voltage $V_{th}$ between transistors utilizing metals and metal alloys having higher silicidation temperature, such as Co (plotted as triangles) and those utilizing metals having lower silicidation temperatures, such as a nickel alloy (plotted as $\circ$ and $\square$) processed at about 500 °C. Indeed, the $V_{th}$ data plotted in FIGS. 9A-B tend to reflect the substantially identical NMOS and PMOS threshold voltages obtained for both $CoSi_2$ and NiSi silicides, indicating the impact of the dopant deactivation during the SBL processing silicidation temperature. This conclusion is reinforced by the data presented in FIGS. 10A-B, which plot the C-V curves for gate oxide capacitors manufactured with both $CoSi_2$ and NiSi silicides that did not receive the conventional the SBL processing. Particularly when compared with the corresponding graphs illustrated in FIGS. 8A-B, the degradation in

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performance resulting from the dopant deactivation is clearly reflected in both the NMOS and PMOS data.

[0054]    As illustrated in FIGS. 11A-B, a comparison of gate oxide capacitors with Ni-silicide manufactured using the conventional process according to FIG. 1 (plotted as □), the conventional process without the SBL step (plotted as △) and an exemplary embodiment of the present invention including a post-SBL anneal (plotted as ○) illustrates the utility of the post-SBL anneal to reactivate the dopant. This result is reflected in the substantial uniformity of the C-V curves generated for the SBL-less process and the post-SBL anneal process, both of which demonstrate capacitance greater than that obtained by the conventional process.

[0055]    As illustrated in FIGS. 12A-B, a comparison of the drain saturation current, $I_{dsat}$, and the drain off current, $I_{doff}$, for both NMOS and PMOS transistors having Ni-silicide manufactured using the conventional process according to FIG. 1, the conventional process without the SBL step (plotted as □) and an exemplary embodiment of the present invention including a post-SBL anneal (plotted as △) further illustrates the utility of the post-SBL anneal to reactivate the dopant. As illustrated by the respective plots, the $I_{dsat}$ at a given $I_{doff}$ level for transistors according to the present invention is increased relative to the conventional method. At an $I_{doff}$ of 10nA, for example, the NMOS transistors manufactured according to the present invention illustrate an improvement of about 5% in the activated dopant.

[0056]    As illustrated in FIGS. 13A-B, by avoiding the dopant deactivation associated with the SBL process, transistors incorporating a Ni-silicide (plotted as ○ and □) may be produced with electrical performance, specifically $I_{dsat}$, that is substantially the same or improved relative to similar Co-silicide transistors (plotted as triangles). Utilizing an exemplary embodiment of the process according to the

present invention, by reactivating a portion of the dopant "lost" during the SBL

process, permits the use of metals and metal alloys having lower silicidation

temperatures, such as nickel and nickel alloys, that may be processed at temperatures

below about 700 °C.

[0057]    While the present invention has been particularly shown and

described with reference to exemplary embodiments thereof, it will be understood by

those of ordinary skill in the art that various changes in form and details may be made

therein without departing from the spirit and scope of the invention as defined by the

appended claims and their equivalents. Silicide can be formed only on source/drain or

only on gate. And the present invention can be applied to make total gate silicidation.